REMARKS

Claims 47-48 and 50 were previously pending in this application. In the interest of expediting prosecution, the Applicants are canceling those claims, without prejudice or disclaimer, and are incorporating them into independent Claim 46. Thus, Claims 46, 49, and 51-62 are pending in the application. Claim 46 has been amended to more precisely claim the disclosed invention. Support for the amendments can be found in the Applicant's Specification on at least page 2, lines 11-13; page 5, lines 5-8 and lines 13-29; page 6, lines 12-21; page 14, lines 13-20; and Figs. 1 and 2.

Examiner Interview

Applicant's Attorney thanks Examiner Wilson for a helpful telephonic interview on November 13, 2006 with the undersigned regarding the pending case. During that interview, U.S. Patent No. 5,524,265 to Balmer was briefly discussed. The examiner also raised concern about the utility of the invention as claimed. The claims have been amended to address that concern.

Rejections under 35 U.S.C. 103(a)

Claims 46, 49, and 51-62 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Balmer (U.S. Patent No. 5,524,265).

To establish a prima facie case for obviousness under 35 U.S.C. 103(a), (1) there must be some suggestion or motivation to modify the reference teachings, (2) there must be a reasonable expectation of success, and (3) the reference must teach or suggest all the claim limitations. For the reasons discussed below, it is respectfully submitted that the Office has not established a prima facie case under 35 U.S.C. 103(a) for Claims 46, 49, and 51-62, and that, therefore, those claims are in condition for allowance.

Before discussing the cited reference, however, a brief review of the Applicant's disclosure may be helpful. The Applicant's disclosed invention is directed to a method of processing data packets in a switch. In reference to Figs. 1 and 3, data packets 126 are received on an ingress port 132 of a switch 100. The data packets 126 are written to buffer memory 108

of the switch 100, and a plurality of pointers 128, 306 to the data packets 126 are enqueued on a first cache memory 302 of an egress port queue 124 of the switch 100. The plurality of data packet pointers 128, 306 in the first memory 302 are transferred to a second memory 300, which is significantly slower than the first memory 302, of the egress port queue 124 in a single transfer cycle by transferring a cache row 304. A single transfer cycle is measured by a single read of the first memory 302. Cache rows of pointers received in successive transfer cycles are linked in a linked list in the second memory 300 as shown in Fig. 5. Each pointer 128, 306 is then dequeued from the second memory 300 and the data packets 126, to which the pointers 128, 306 point, are forwarded to a destination 112.

In reference to Figs. 1 and 2, one embodiment of the present invention provides that in a switch 100 that comprises an ingress port 132 and a plurality of egress ports 130a-e, a plurality of data packet pointers 128, 306 (one for each egress port 130a-e) may be enqueued on the plurality of egress ports 130a-e in respective egress port queues 124a-e in a single port cycle 200a. On subsequent port cycles 200b-f, only one data packet pointer 128, 306 is dequeued from a single egress port queue 124. Thus, an enqueue cycle time 202 is significantly faster than a dequeue cycle time 200. Since the number of ports that a switch may support is limited by the speed at which the location of the data packets in the buffer memory can be enqueued on an egress port queue, the present invention allows the switch to support a greater number of ports while limiting the cost of and the space consumed by the memories of the egress port queues.

With regard to the cited prior art, Balmer discusses a data transfer controller for transferring data between memories of multiple processors. Balmer does not teach or suggest the use of a first memory and a second memory having significantly different access times as claimed by the Applicants in Claim 46. The examiner states on page 2 of the Office Action that while Balmer does not expressly call for a second memory having a different access time from a first memory, the memories are in two different processors. The examiner appears to contend that different processors inherently have different access times, though designed for a common access time. The memories of the Applicant's claimed invention, however, should be interpreted as having nominally different access times, that is, more than a minute difference in access times. While Balmer teaches the use of memories that are in two different processors, the memories of the processors are not intended to have different access times. For instance, Balmer notes that

the data transfer controller "preferably includes plural identical processors" (*See* Balmer, col. 9, lines 49-60.)

Furthermore, Balmer does not teach or suggest "a second memory access time that is significantly slower than the first memory access time" as now claimed by the Applicants in Claim 46. The examiner appears to contend that Balmer's use of a linked list or parallel data transfer follows from Balmer's source (or first) memory having an access time that is less than its destination (or second) memory. As discussed above, the circuit of Balmer preferably includes plural identical processors; therefore, Balmer does not teach or suggest that the second memory access time is significantly slower than the first memory access time.

Furthermore, Balmer does not teach or suggest that a plurality of pointers is transferred "in a single transfer cycle" as now claimed by the Applicants in Claim 46. The examiner states that while Balmer does not expressly call for transferring a plurality of pointers in a single transfer cycle, that Balmer's process of transferring all the elements of a linked list from one processor to another defines a transfer cycle. According to the Applicant's Specification, a "transfer cycle" is measured by a single read of the first memory. Thus, in a single read of the first memory, a plurality of pointers is transferred from the first memory to the second memory (*See* Applicant's specification, page 8, lines 18-27.) In contrast, Balmer does not transfer a plurality of pointers in a single read of its source (or first) memory, but transfers one packet at a time from its source (or first) memory to its destination (or second) memory (*See* Balmer, col. 56, lines 1-20.) Moreover, the elements of the linked lists of Balmer are transferred in a round robin fashion while existing transfers are suspended by intervening transfers (*See* Balmer, col. 72, lines 1-42.)

Furthermore, Balmer does not teach or suggest "dequeuing each pointer from the second memory as the data packets are forwarded by the egress port" as now claimed by the Applicants in Claim 46. The examiner states that while Balmer does not expressly call for dequeuing each pointer from the destination (or second) memory, Balmer replaces existing linked lists with new linked lists, and by doing so, must dequeue the previous linked lists; but Balmer merely transfers data from a source memory to a destination memory. At best, Balmer would dequeue elements of a linked list from the source (or first) memory; there is no suggestion of dequeuing pointers from the destination (or second) memory (*See* Balmer, col. 54, line 41 – col. 56, line 48.)

Therefore, Balmer does not teach or suggest the Applicant's invention as now claimed in independent Claim 46. Accordingly, the Applicants respectfully submit that the rejection of Claim 46 under 35 U.S.C. 103(a) as being unpatentable over Balmer should be withdrawn.

Dependent claims 49 and 51-62 should be found in allowable condition for the same reasons as Claim 46 above, as well as on the basis of additional limitations in these claims.

As such, the 35 U.S.C. 103(a) rejections of Claims 46, 49, and 51-62 are believed to be overcome. Accordingly, the present invention as claimed is not believed to be made obvious from the cited art or any of the prior art. Removal of the rejections under 35 U.S.C. 103(a) and acceptance of Claims 46, 49, and 51-62 is respectfully requested.

Information Disclosure Statement

A copy of the Information Disclosure Statement (IDS) as filed on March 20, 2002 and references are being filed concurrently herewith, in response to the Examiner's statement (Office Action, page 9, part 5) that the list of references and copies of the cited references were not provided. Entry of the IDS is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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